**FPGA HW/SW Codesign Approach for Real-time Image Processing Using HLS**

* Real-time constraint is one of the most common challenge found in many critical embedded applications, namely image and video processing. Recently, FPGA reconfigurable circuit with its HLS software tools is become a very promising technology to be widely used in many applications encompassing all aspects and requirements of embedded system.
* The processing complexity of these restrictive algorithms make their implementation on conventional general purpose processors not feasible and are best suited to hardware implementation. Because the h/w circuits have intrinsic properties namely pipeline & parallelism.
* This work addresses the implementation of image and video processing algorithms like morphological and convolution operation on FPGA using co-design approach and HLS Vivado tools, in which the objective is to show the feasibility of designing critical embedded applications on FPGA platform by using HW/SW co-design approach and high-level synthesis tools that allow to have a good compromise in terms of performance and development time.
* **The new Xilinx technology Zynq SoC:**
* Zynq consists of two main parts: a Processing System (PS) that is built around a dual-core ARM Cortex-A9 processor and a Programmable Logic (PL) equivalent to hardware accelerator (FPGA)
* There exist different kinds of programming the FPGA zynq device:

Programming the Processing System (Software)

Programming the Programmable Logic (Hardware)

Co-design HW/SW programming (PL/PS)

* Zedboard platform can serves as a unique platform for Embedded system design as well as hardware/software co-design.
* The different algorithms implemented on co-design will be shown and compared them with other purely software implementation.
* **Convolution algorithm:**
* The convolution operation requires, for an iteration, a certain number of pixels for it to be performed (convolution window), these pixels will be received by the hardware structure, which will handle the convolution, through the part software.
* The values of the buffers will be then multiplied by the convolution mask, pixel by pixel, and the result will be stored in another window, having the same size as the mask, the operation that will be chosen, the IP proceeds to a certain number of methods to return to the output the value of the appropriate pixel:

**Convolution:** We perform the pixel-by-pixel sum of the resulting window, and the value of the sum will be returned.

**Erosion:** extract the maximum value of the resulting window and it will be returned.

**Dilation:** extract the minimum value of the resulting window and it will be returned.

* The results demonstrate that the proposed codesign approach for image and video processing through a convolution design require a low FPGA resources in terms of LUT

(9 %) BRAM (3 %) and FF (5 %).

* In the software implementation, hardware implementation is usually required as a material accelerator to provide high processing speed. However, hardware approach require a long prototyping time. Therefore, co-design approach presents a good compromise between performances and prototyping time